EC45

NEW SCHEME

USN ☐☐☐☐☐☐☐☐☐☐

Fourth Semester B.E. Degree Examination, January/February 2005

BM/EC/EE/TE/ML/IT

Microprocessors

Time: 3 hrs.]

[Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) What is a microprocessor? Write and explain the architecture of 8085.
   (10 Marks)

   (b) Explain the following instructions and indicate flags affected.

   i) DAA   ii) DAD D
   iii) XCHG   iv) HALT
   v) MOV M, A

   (10 Marks)

2. (a) Explain the operation of the following pins of 8085

   i) Clockout   ii) SID
   iii) HOLD   iv) TRAP
   v) AD0-AD_7

   (10 Marks)

   (b) Write a single instruction equivalent of 8085 to program sequence shown below
   :

i)	POP B	ii)	LXI B 2050
	MOV E, L		MOV A, L
	MOV D, H		STA X B
	MOV L, C		INXB
	MOV H, B		MOV A, H
	PUSH D		STA X B

   (8 Marks)

   (c) How is the address - data bus of 8085 demultiplexed? **(2 Marks)**

3. (a) Write an ALP for 8085 processor to separate ODD and EVEN numbers from an array of 16 numbers stored from F100. Store the even numbers from F120, and odd numbers from FI50. **(10 Marks)**

   (b) List out differences and similarities between CALL - RET and PUSH -POP instructions. **(10 Marks)**

4. (a) Draw the timing diagram for the instruction STA 8000. **(10 Marks)**

   (b) Determine the length of 2 strings of ASCII characters. The END of the string is marked by a carriage return character ('CR' hex code OD). Write the sub routine to determine the length of string. If string lengths are equal store FF else 00 in accumulator. **(10 Marks)**

5. (a) Differentiate between I/O mapped I/O and memory mapped I/O.   (8 Marks)

     (b) Interface 8K bytes of EPROM & 4K bytes of RAM, 8 I/P devices, 8 O/P devices to a 8085 system in I/O mapped I/O. The memories are provided in 2K bytes ICs. Give the schematic diagram with address data bus demultiplexing, indicating the decoding logic & the address space for each.   (12 Marks)

6. (a) Distinguish between :

       i)   Vectored and Non vectored interrupt

       ii)   Maskable and non maskable interrupt

       iii)   Internal and external interrupt

       iv)   Software and hardware interrupt.   (8 Marks)

     (b) Explain in detail the *mode | I | P port and O/P port* handshaking signals of 8255.   (8 Marks)

     (c) Write an ALP to generated square wave duty cycle using 8255.   (4 Marks)

7. (a) What are different modes of operation of 8253? Explain mode '0' and model '1' with timing diagram.   (8 Marks)

     (b) Write the signals of RS-232 port.   (3 Marks)

     (c) Write & explain the mode word format, command word format & status word format of 8251.   (9 Marks)

8. (a) Describe the features of 8279 with its block diagram.   (10 Marks)

     (b) Write short notes on :

       i)   DMA controller

       ii)   Interrupt operation of 8259   (10 Marks)

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